



AD9361-CSL Data Sheet Revision

AD9361 CS DS Header (Rev. A vs Rev. B)

AD9361S-CSL REVA

AD9361-CSL REVB



Commercial Space
Product

Data Sheet
AD9361S-CSL

RF Agile Transceiver



Commercial Space
Product

Data Sheet
AD9361-CSL

RF Agile Transceiver

AD9361 Features

AD9361S-CSL Rev A

FEATURES

- ▶ RF 2 × 2 transceiver with integrated 12-bit DACs and ADCs
- ▶ Transmit band: 46.875 MHz to 6.0 GHz
- ▶ Receive band: 70 MHz to 6.0 GHz
- ▶ Dual receivers: 6 differential or 12 single-ended inputs
- ▶ Superior receiver sensitivity with a NF of 2 dB at 800 MHz LO
- ▶ Receive gain control
 - ▶ Real-time monitor and control signals for manual gain
 - ▶ Independent AGC
- ▶ Dual transmitters: 4 differential outputs
- ▶ Highly linear broadband transmitter
 - ▶ Transmit EVM: -40 dB (typical) at 800 MHz
 - ▶ Transmit noise: -157 dBm/Hz (typical)
 - ▶ Transmit monitor: 66 dB dynamic range (typical) with 1 dB accuracy
- ▶ Integrated fractional-N synthesizers
 - ▶ 2.4 Hz typical LO frequency step size
- ▶ Multichip synchronization
- ▶ CMOS/LVDS digital interface

AD9361-CSL Rev B

FEATURES

- ▶ RF 2 × 2 transceiver with integrated 12-bit DACs and ADCs
- ▶ Transmit band: 46.875 MHz to 6.0 GHz
- ▶ Receive band: 70 MHz to 6.0 GHz
- ▶ Dual receivers: 6 differential
- ▶ Superior receiver sensitivity with a NF of 2 dB at 800 MHz LO
- ▶ Receive gain control
 - ▶ Real-time monitor and control signals for manual gain
 - ▶ Independent AGC
- ▶ Dual transmitters: 4 differential outputs
- ▶ Highly linear broadband transmitter
 - ▶ Transmit EVM: -40 dB (typical) at 800 MHz
 - ▶ Transmit noise: -157 dBm/Hz (typical)
 - ▶ Transmit monitor: 66 dB dynamic range (typical) with 1 dB accuracy
- ▶ Integrated fractional-N synthesizers
 - ▶ 2.4 Hz typical LO frequency step size
- ▶ Multichip synchronization
- ▶ CMOS/LVDS digital interface

AD9361 Commercial Features

AD9361S-CSL Rev A

COMMERCIAL SPACE FEATURES

- ▶ Wafer diffusion lot traceability
- ▶ Radiation lot acceptance testing: TID

AD9361-CSL Rev B

COMMERCIAL SPACE FEATURES

- ▶ Supports aerospace applications
- ▶ Certificate of Conformance
- ▶ Wafer diffusion lot traceability
- ▶ Qualification based on flows per NASA PEM-INST-001 and SAE AS6294
- ▶ Burn-in, life test, and deltas analysis
- ▶ Radiation lot acceptance test (RLAT)
 - ▶ Total ionizing dose (TID)
- ▶ Radiation benchmark
 - ▶ No single event latch-up (SEL) occurs at effective linear energy transfer (LET): $\leq 80 \text{ MeV-cm}^2/\text{mg}$
- ▶ Outgassing characterization

AD9361 Applications

AD9361S-CSL Rev A

APPLICATIONS

- ▶ Low Earth orbit (LEO) satellites
- ▶ Avionics
- ▶ Point to point communication systems

AD9361-CSL Rev B

APPLICATIONS

- ▶ Low and Medium Earth Orbit (LEO/MEO) satellites
- ▶ Avionics
- ▶ Point to point communication systems

AD9361 General Description

AD9361S-CSL Rev A

GENERAL DESCRIPTION

The **AD9361S-CSL** is a high performance, highly integrated, RF agile transceiver designed for use in 3G and 4G applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The **AD9361S-CSL** receiver LO operates from 70 MHz to 6.0 GHz and the transmitter LO operates from 46.875 MHz to 6.0 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported.

The two independent direct conversion receivers have state-of-the-art noise figure and linearity. Each receive subsystem includes independent automatic gain control (AGC), dc offset correction, quadrature correction, and digital filtering, thereby eliminating the need for these functions in the digital baseband. The AD9361S-CSL also has flexible manual gain modes that can be externally controlled.

Two high dynamic range analog-to-digital converters (ADCs) per channel digitize the received inphase (I) and quadrature (Q) signals and pass them through configurable decimation filters and 128-tap finite impulse response (FIR) filters to produce a 12-bit output signal at the appropriate sample rate.

The transmitters use a direct conversion architecture that achieves high modulation accuracy with ultralow noise. This transmitter design produces a best-in-class transmit error vector magnitude (EVM) of ≤ -40 dB, allowing significant system margin for the external power amplifier (PA) selection. The on-board transmit power monitor can be used as a power detector, enabling highly accurate transmit power measurements.

The fully integrated phase-locked loops (PLLs) provide low power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation, demanded by frequency division duplex (FDD) systems, is integrated into the design. All voltage controlled oscillator (VCO) and loop filter components are integrated.

The **AD9361S-CSL** is packaged in a 10 mm \times 10 mm, 144-ball chip scale package ball grid array (CSP_BGA).

Additional application and technical information can be found in the [Commercial Space Products Program](#) brochure and the **AD9361** data sheet.

AD9361-CSL Rev B

GENERAL DESCRIPTION

The **AD9361-CSL** is a high performance, highly integrated, RF agile transceiver designed for use in 3G and 4G applications. Its programmability and wideband capability make it ideal for a broad range of transceiver applications. The device combines an RF front end with a flexible mixed-signal baseband section and integrated frequency synthesizers, simplifying design-in by providing a configurable digital interface to a processor. The **AD9361-CSL** receiver LO operates from 70 MHz to 6.0 GHz and the transmitter LO operates from 46.875 MHz to 6.0 GHz range, covering most licensed and unlicensed bands. Channel bandwidths from less than 200 kHz to 56 MHz are supported.

The two independent direct conversion receivers have state-of-the-art noise figure and linearity. Each receive subsystem includes independent automatic gain control (AGC), dc offset correction, quadrature correction, and digital filtering, thereby eliminating the need for these functions in the digital baseband. The AD9361-CSL also has flexible manual gain modes that can be externally controlled.

Two high dynamic range analog-to-digital converters (ADCs) per channel digitize the received inphase (I) and quadrature (Q) signals and pass them through configurable decimation filters and 128-tap finite impulse response (FIR) filters to produce a 12-bit output signal at the appropriate sample rate.

The transmitters use a direct conversion architecture that achieves high modulation accuracy with ultralow noise. This transmitter design produces a best-in-class transmit error vector magnitude (EVM) of ≤ -40 dB, allowing significant system margin for the external power amplifier (PA) selection. The on-board transmit power monitor can be used as a power detector, enabling highly accurate transmit power measurements.

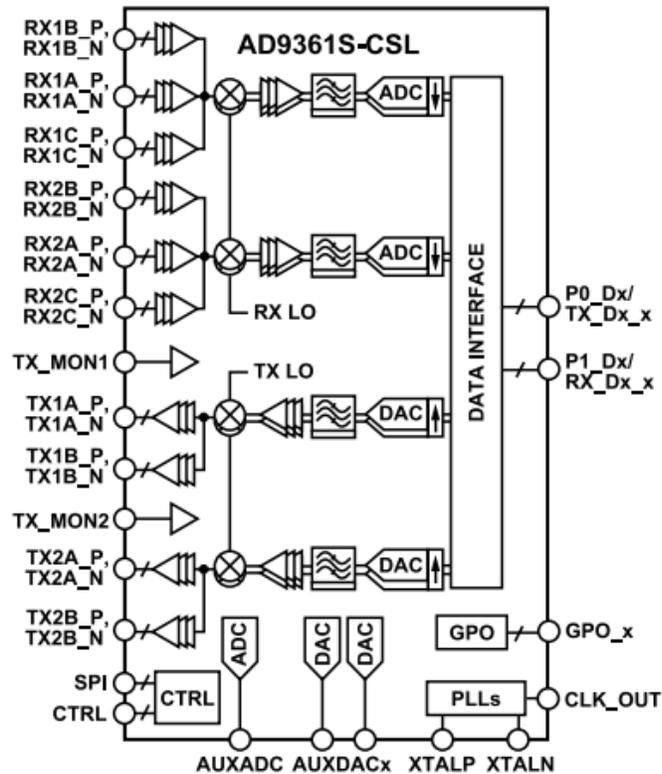
The fully integrated phase-locked loops (PLLs) provide low power fractional-N frequency synthesis for all receive and transmit channels. Channel isolation, demanded by frequency division duplex (FDD) systems, is integrated into the design. All voltage controlled oscillator (VCO) and loop filter components are integrated.

The **AD9361-CSL** is packaged in a 10 mm \times 10 mm, 144-ball chip scale package ball grid array (CSP_BGA).

Additional application and technical information can be found in the [Commercial Space Products Program](#) brochure and the **AD9361** data sheet.

AD9361 Figure 1

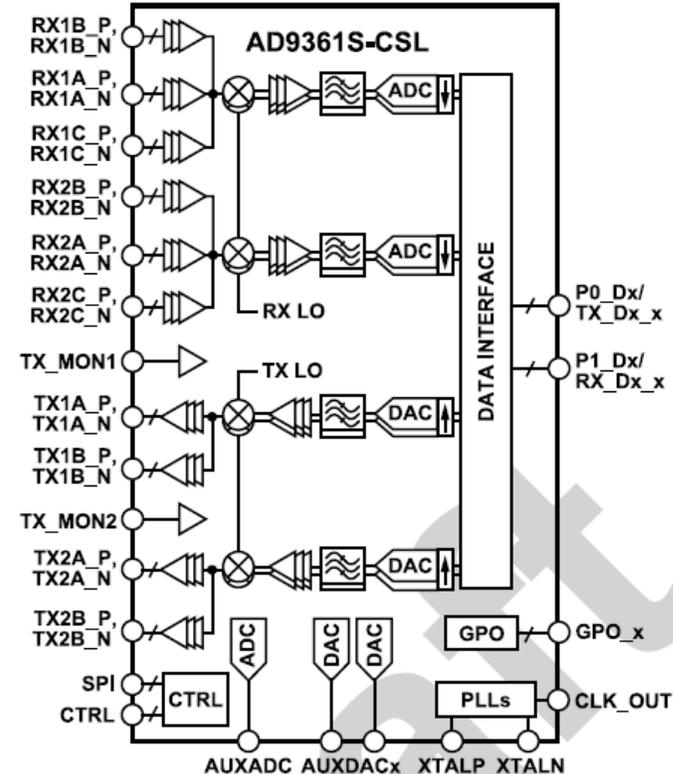
AD9361S-CSL Rev A



NOTES
 1. SPI, CTRL, P0_Dx/TX_Dx_x, P1_Dx/RX_Dx_x, AND GPO_x CONTAIN MULTIPLE PINS.

Figure 1.

AD9361-CSL Rev B



NOTES
 1. SPI, CTRL, P0_Dx/TX_Dx_x, P1_Dx/RX_Dx_x, AND GPO_x CONTAIN MULTIPLE PINS.

Figure 1. Functional Block Diagram

AD9361 Specs Table

AD9361S-CSL Rev A

AD9361-CSL Rev B

SPECIFICATIONS

Table 1. (Continued)

Parameter ¹	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
REFERENCE CLOCK						The reference clock is either the input to the XTALP/XTALN pins or a line directly to the XTALN pin
Input						
Frequency Range		19		50	MHz	Crystal input
		10		80	MHz	External oscillator
Signal Level			1.3		V p-p	AC-coupled external oscillator

SPECIFICATIONS

Table 1. (Continued)

Parameter ¹	Symbol	Min	Typ	Max	Unit	Test Conditions/ Comments
REFERENCE CLOCK						The reference clock is either the input to the XTALP/XTALN pins or a line directly to the XTALN pin
Input						
Frequency Range		19		50	MHz	Crystal input
		20		80	MHz	External oscillator
Signal Level		0.8		1.3	V p-p	AC-coupled external oscillator. Larger swings close to max level give best performance.

AD9361 Radiation Features Table

AD9361-CSL Rev B Page 17

RADIATION FEATURES

Table 15. Radiation Features

Specifications	Value	Unit
Maximum Total Dose Available (Dose Rate = 50 rad(Si)/s to 300 rad(Si)/s) ¹	30	krad(Si)
No Single Event Latch-Up (SEL) Occurs at Effective Linear Energy Transfer (LET) ²	≤80	MeV-cm ² /mg

¹ Guaranteed by device and process characterization. Contact Analog Devices for data available up to 30 krad.

² Limits are characterized at initial qualification and after any design or process changes that may affect the SEL characteristics, but are not production lot tested unless specified by the customer through the purchase order or contract. For more information on single event effect (SEE) test results, contact Analog Devices for further data beyond published report on the Analog Devices website.

AHEAD OF WHAT'S POSSIBLE

analog.com

